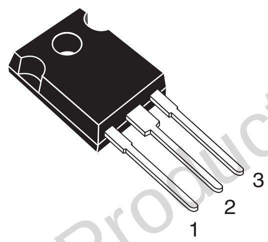
STGW50NC60W

N-channel 600V - 55A - TO-247
Ultra fast switching PowerMESH™ IGBT

Features

Type	V_{CES}	$V_{CE(sat)}$ (max)@25°C	I_C @100°C
STGW50NC60W	600V	< 2.6V	55A

- Very high frequency operation
- Low C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)



TO-247

Applications

- Very high frequency inverters, UPS
- HF, SMPS and PFC in both hard switch and resonant topologies
- Motor drivers
- Welding

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “W” identifies a family optimized for very high frequency applications.

Figure 1. Internal schematic diagram

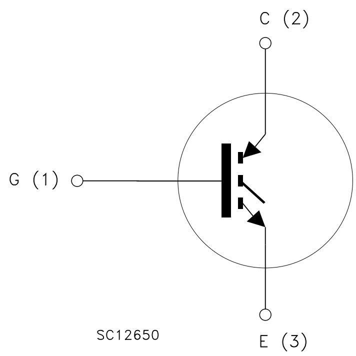


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW50NC60W	GW50NC60W	TO-247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C (1)	Collector current (continuous) at T_C = 25°C	100	A
I_C (1)	Collector current (continuous) at T_C = 100°C	55	A
I_{CL} (2)	Turn-off SOA minimum current	250	A
V_{GE}	Gate-emitter voltage	±20	V
P_{TOT}	Total dissipation at T_C = 25°C	285	W
T_j	Operating junction temperature	-55 to 150	°C

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. V_{clamp} = 480V, T_J=150°C, R_G=10Ω, V_{GE}=15V

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max IGBT	0.45	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C= 1mA, V_{GE}= 0	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15V, I_C= 40A V_{GE}= 15V, I_C=40A,Tc=125°C		2.1 1.9	2.6	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250µA	3.75		5.75	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE}= Max rating,T_C= 25°C V_{CE}= Max rating,T_C= 125°C			500 5	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE}= ±20V, V_{CE}= 0			±100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C=40A		25		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1MHz, V_{GE} = 0		4700 410 90		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 40A, V_{GE} = 15V, *Figure 16*		195 32 82		nC nC nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V		52 17 2400		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V, Tj = 125°C		50 19 2020		ns ns A/µs
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V,		31 240 35		ns ns ns
$t_{r(Voff)}$ $t_{d(Voff)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V, Tj = 125°C		59 280 63		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on} E_{off}(1) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V, *Figure 15*		365 560 925	470 790 1260	µJ µJ µJ
E_{on} E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 40A R_G= 10Ω, V_{GE}= 15V, Tj = 125°C *Figure 15*		635 910 1545		µJ µJ µJ

1. Turn-off losses include also the tail of the collector current

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

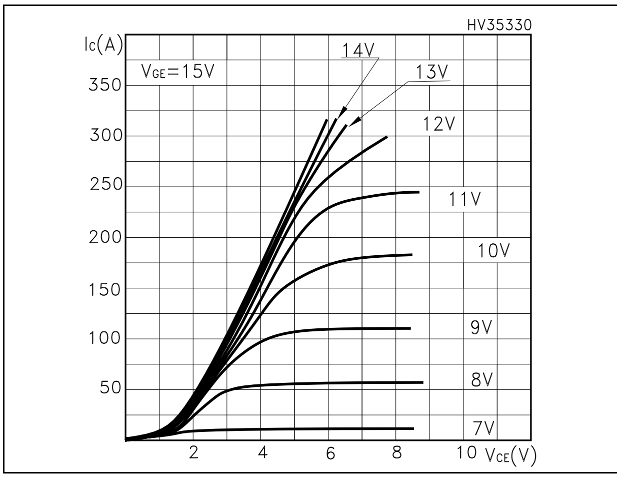


Figure 2. Transfer characteristics

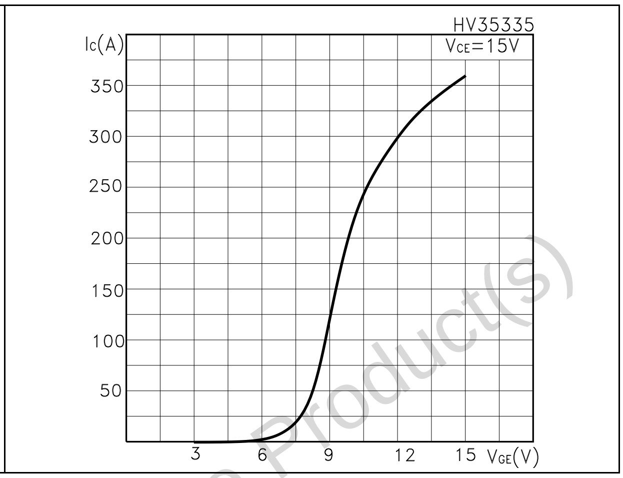


Figure 3. Transconductance

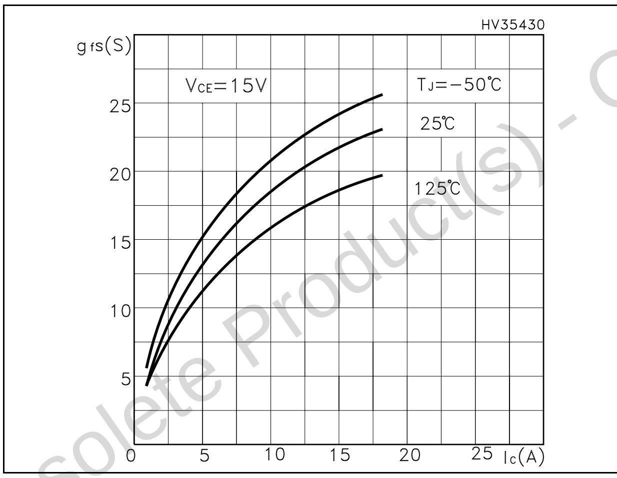


Figure 4. Collector-emitter on voltage vs temperature

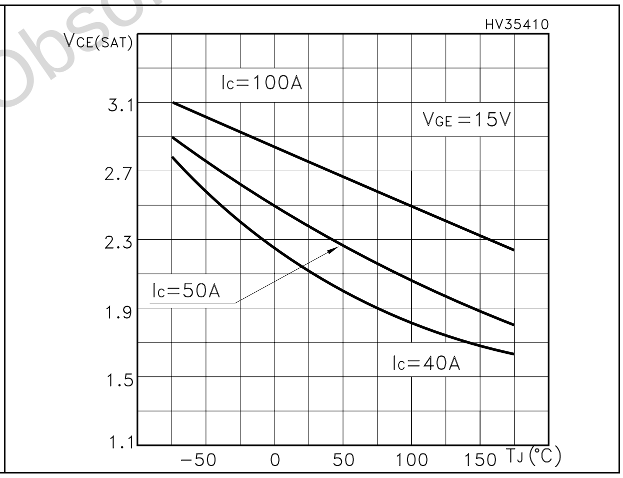


Figure 5. Gate charge vs gate-source voltage

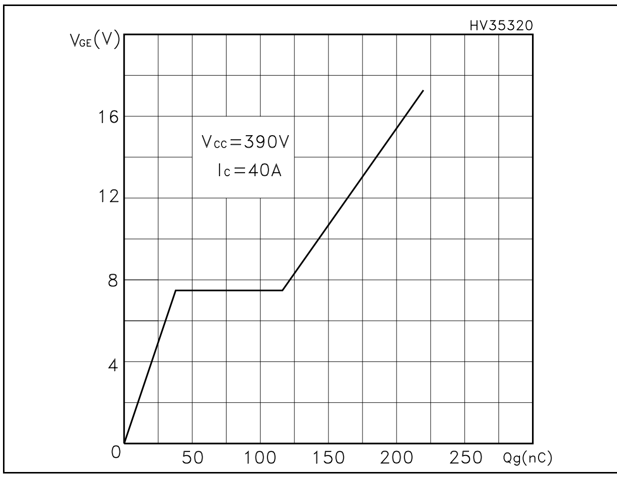


Figure 6. Capacitance variations

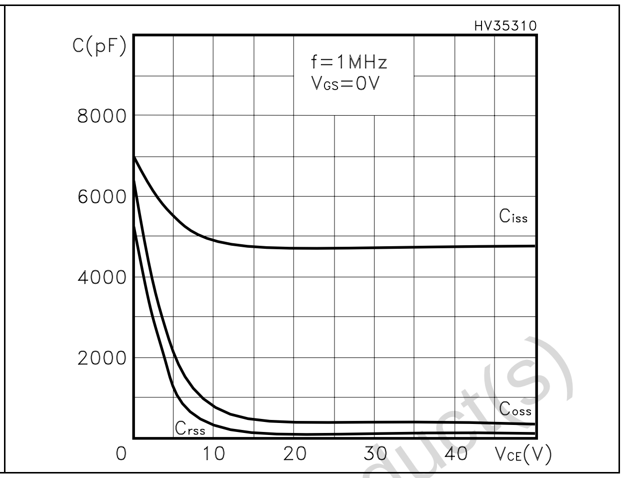


Figure 7. Normalized gate threshold voltage vs temperature

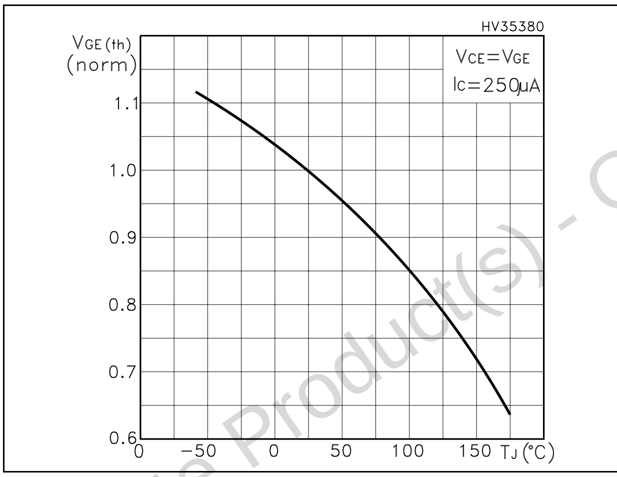


Figure 8. Collector-emitter on voltage vs collector current

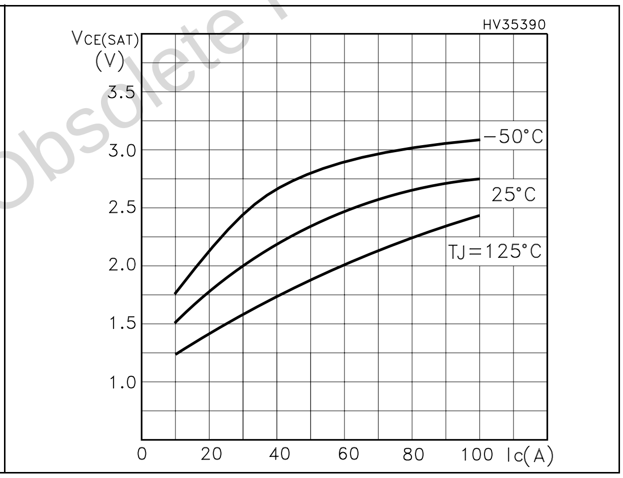


Figure 9. Normalized breakdown voltage vs temperature

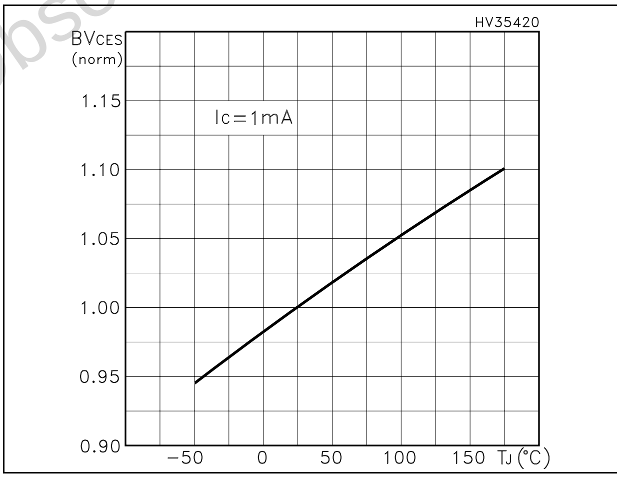
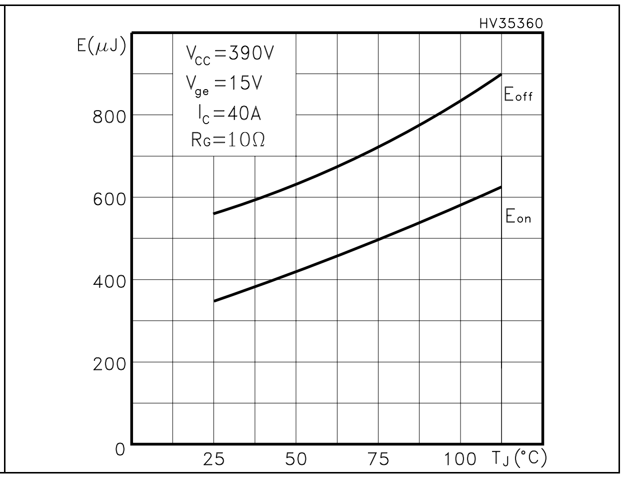


Figure 10. Switching losses vs temperature



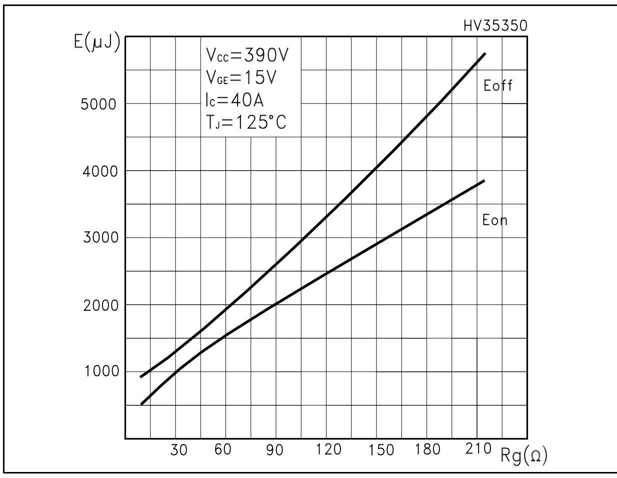


Figure 11. Switching losses vs gate resistance

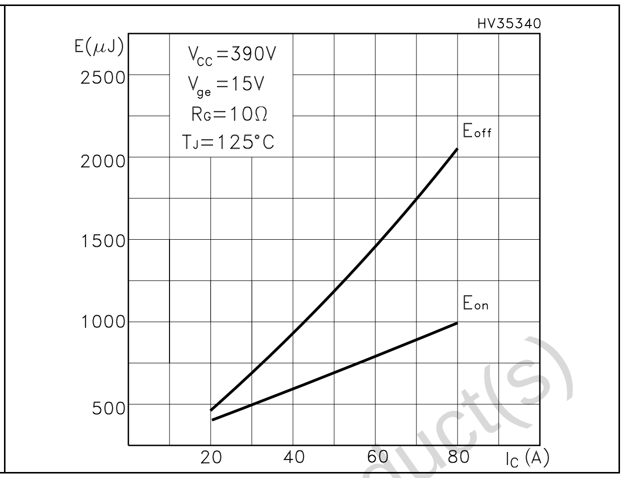


Figure 12. Switching losses vs collector current

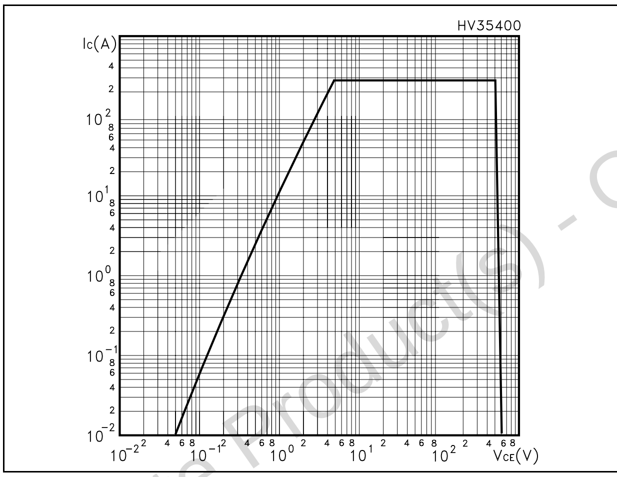


Figure 13. Turn-off SOA

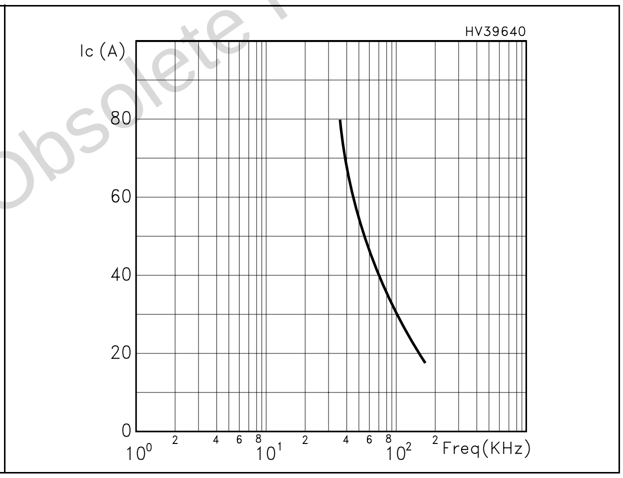


Figure 14. I_C vs. frequency

2.2 Frequency applications

For a fast IGBT suitable for high frequency applications, the typical collector current vs. maximum operating frequency curve is reported. That frequency is defined as follows:

$f_{MAX} = (P_D - P_C) / (E_{ON} + E_{OFF})$

- The maximum power dissipation is limited by maximum junction to case thermal resistance:

Equation 1

$P_D = \Delta T / R_{THJ-C}$

considering $\Delta T = T_J - T_C$ = 125 °C- 75 °C = 50°C

- The conduction losses are:

Equation 2

$P_C = I_C * V_{CE(SAT)} * \delta$

with 50% of duty cycle, V_{CESAT} typical value @125°C.

- Power dissipation during ON & OFF commutations is due to the switching frequency:

Equation 3

$P_{SW} = (E_{ON} + E_{OFF})$ * freq.

- Typical values @ 125°C for switching losses are used (test conditions: V_{CE} = 390V, V_{GE} = 15V, R_G = 10 Ohm). Furthermore, diode recovery energy is included in the E_{ON} (see note 2), while the tail of the collector current is included in the E_{OFF} measurements (see note 3).

3 Test circuit

Figure 15. Test circuit for inductive load switching

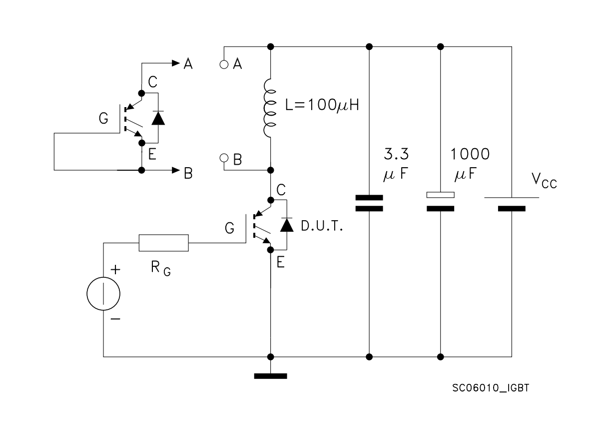
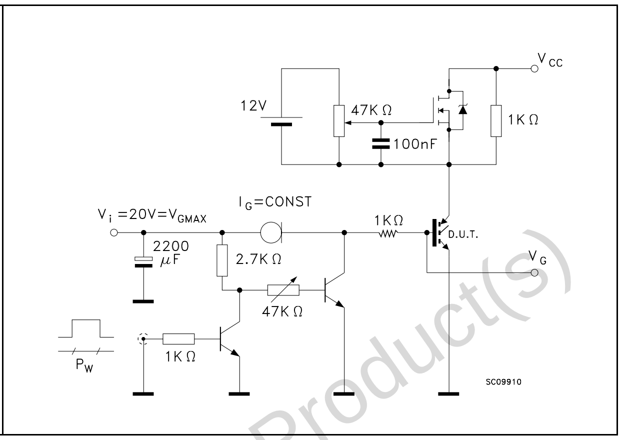


Figure 16. Gate charge test circuit

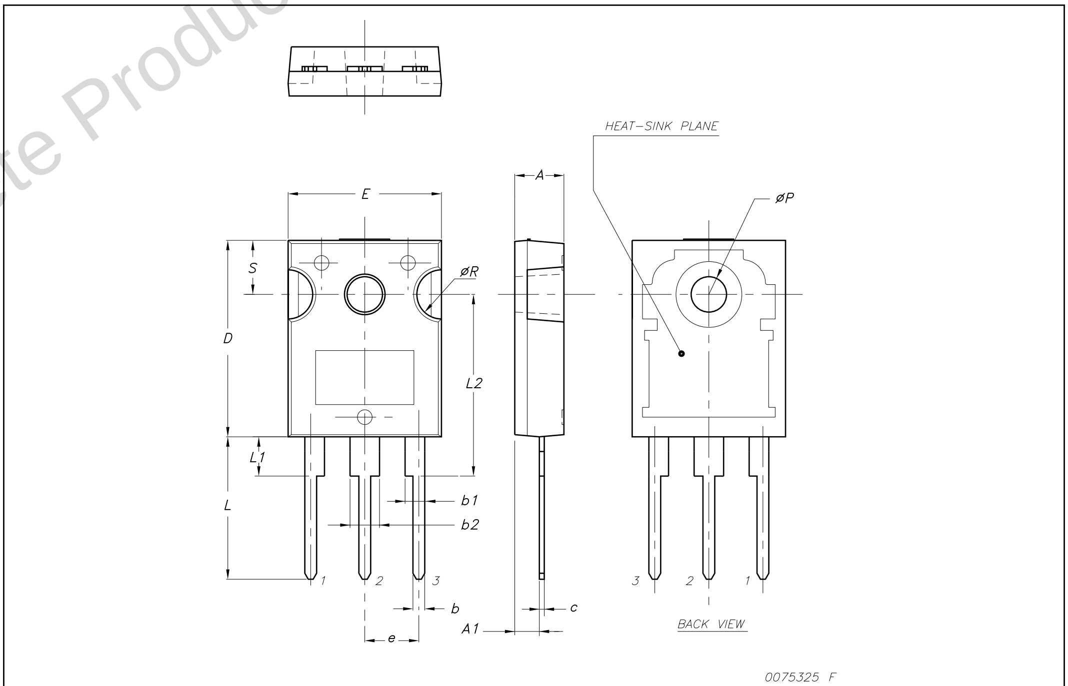


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
24-Aug-2007	1	Initial release.

STMicroelectronics group of companies

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